

REMARKS

Claims 1-18 are pending in the present application. Claims 1, 7 and 13 have been amended.

Drawings

Applicant notes that the drawings had been objected to in the previous Office Action dated November 7, 2002. As noted in the Amendment dated January 21, 2003, the specification has been corrected on page 11 to generally describe formation of a fifth diffusion layer 211 in first diffusion layer 203. The drawings thus are believed to be in compliance with 37 C.F.R. 1.84(p)(5). **The Examiner is respectfully requested to acknowledge on the record that the drawings as filed along with the present application are accepted.**

Claim Rejections-35 U.S.C. 112

Claims 1-18 have been rejected under 35 U.S.C. 112, second paragraph, for the reasons stated on page 2 of the current Office Action dated April 7, 2003. Claims 1, 7 and 13 have been amended to provide clearer antecedent basis for "said forming the gate oxide layer", as requested by the Examiner. However, in order to avoid consideration of claim scope in terms of step plus function under the sixth paragraph of 35 U.S.C. 112, "step" has not been inserted into the claims as suggested by the Examiner. Applicant respectfully submits that claims 1, 7 and 13 are in compliance with

35 U.S.C. 112, second paragraph, and thus respectfully urges the Examiner to withdraw this rejection.

Claim Rejections-35 U.S.C. 102

Claims 1, 5-7, 11-13, 17 and 18 have been rejected under 35 U.S.C. 102(a) as being anticipated by the Efland et al. reference (U.S. Patent No. 6,137,140). This rejection is respectfully traversed for the following reasons.

The method of manufacturing an LDMOS transistor of claim 1 includes in combination "implanting ions of the first conductivity type into a part of the well region" and "forming a gate oxide layer on the surface of the semiconductor substrate", said forming the gate oxide layer "including subjecting the semiconductor substrate to a heat treatment so that the implanted ions are diffused to form a diffusion region of the first conductivity type on the surface of the semiconductor substrate". As further featured, said implanting ions "is carried out with an energy set so that an accelerated oxidation during said forming the gate oxide layer is inhibited". Applicant respectfully submits that the Efland et al. reference as relied upon by the Examiner does not disclose these features.

Applicant initially emphasizes that said forming a gate oxide layer of claim 1 necessarily occurs **subsequent** to said implanting ions, because the heat treatment performed during said forming the gate oxide layer diffuses the previously implanted ions to form a diffusion region.

On page 3, lines 2-3 of the current Office Action dated April 7, 2003, the

Examiner has alleged that column 3, lines 26-27 of the Efland et al. reference may be interpreted as said implanting ions of claim 1. The Examiner has further alleged on page 3, lines 3-4 of the current Office Action that column 3, lines 23-24 and column 4, lines 13-18 of the Efland et al. reference may be interpreted as said forming a gate oxide layer of claim 1. Applicant respectfully submits that the Examiner's interpretation of the Efland et al. reference with respect to claim 1 is clearly erroneous.

Particularly, the ions implanted into the n⁺ regions as described in column 3, lines 26-27 of the Efland et al. reference occurs after forming of the gate oxide region as described in column 3, lines 23-24 of the Efland et al. reference. Since the ions are implanted after formation of the gate oxide region as described in the relied upon portions of the Efland et al. reference, formation of the gate oxide region clearly does not diffuse the ions that are thereafter implanted in order to form a diffusion region. Clearly, the process of forming the gate oxide region as described in column 3, lines 23-24 of the Efland et al. reference cannot function to diffuse ions which have not yet been implanted. Applicant also emphasizes that column 4, lines 13-18 of the Efland et al. reference as relied upon by the Examiner does not disclose or suggest implanting ions, and subsequently forming a gate oxide layer that functions to diffuse the implanted ions, as would be necessary to meet the features of claim 1. If this rejection is to be maintained, the Examiner is respectfully requested to clearly establish on the record how the Efland et al. reference may be interpreted as firstly implanting ions, and then subsequently forming a gate oxide layer that

functions to diffuse the previously implanted ions.

With further regard to this rejection, the Examiner has alleged on page 3, lines 4-6 of the current Office Action that column 3, lines 23-24 and column 4, lines 13-18 of the Efland et al. reference may be interpreted as forming a gate oxide layer including subjecting the semiconductor substrate to a heat treatment. However, column 3, lines 23-24 and column 4, lines 13-18 of the Efland et al. reference do not disclose or even remotely suggest a heat treatment in connection with forming a gate oxide layer. It would thus appear that the Examiner has impermissibly implied the existence of features in the reference that are not disclosed. **If this rejection is to be maintained, the Examiner is respectfully requested to clearly establish on the record specific description in the Efland et al. reference of a heat treatment in connection with formation of a gate oxide layer, and more particularly a heat treatment during formation of gate oxide layer that diffuses previously implanted ions.**

With further regard to this rejection, the Examiner has alleged on page 3, lines 6-8 of the current Office Action that column 3, lines 26-27 and column 4, line 14 of the Efland et al. reference may be interpreted as diffusing implanted ions to form a diffusion region. However, column 3, lines 26-27 of the Efland et al. reference as relied upon by the Examiner describe **implantation after** formation of the gate oxide region. Column 4, line 14 of the Efland et al. reference merely describes in general a Dwell 33. Accordingly, the Efland et al. reference as relied upon by the Examiner fails to disclose or even remotely suggest forming a gate oxide layer subsequent implanting ions,

whereby a heat treatment during formation of the gate oxide layer diffuses the previously implanted ions.

With further regard to this rejection, the Examiner has very generally alleged on page 3, lines 11-13 of the current Office Action that the Efland et al. reference discloses with respect to Fig. 3 that an "implanting ions step could be carried out with an energy set so that an accelerated oxidation during formation of the gate oxide layer is inhibited to achieve formation of diffusion region 33". However, Applicant respectfully submits that since the Efland et al. reference does not disclose or even remotely discuss or consider setting energy of the implantation as described in column 3, lines 26-27 and/or accelerated oxidation during formation of a gate oxide layer, the Efland et al. reference clearly fails to disclose that such features "could be carried out", as suggested by the Examiner. In absence of disclosure or consideration of setting energy of the implantation and/or accelerated oxidation, the Examiner has clearly relied upon impermissible hindsight to maintain that these features "could be carried out" in the Efland et al. reference. These features are not taught in the reference and thus the Examiner's reliance on the Efland et al. reference under 35 U.S.C. 102 is clearly improper.

On page 4 of the current Office Action dated April 7, 2003, the Examiner has responded to the arguments presented in the Amendment dated January 21, 2003. The Examiner has alleged on page 4, lines 15-18 of the current Office Action that "Efland et al. discloses formation of diffused regions by implantation (Column 1, lines

17-19, Column 3, lines 18-21, and 26-27), and growing a gate oxide thereon, therefore, subjecting the substrate to a heat treatment, diffusing implanted ions". Applicant respectfully submits that column 1, lines 17-19 and column 3, lines 18-21 of the Efland et al. reference merely describe diffusion in general, not formation of a gate oxide layer including a heat treatment that diffuses previously implanted ions. As emphasized previously, the Efland et al. reference does not disclose or even remotely suggest forming a gate oxide layer including a heat treatment.

Additionally, on page 4, lines 18-22 of the current Office Action, the Examiner has relied on specific pages and figures of U.S. provisional application serial no. 60/047,474, apparently in support of the corresponding rejection under 35 U.S.C. 102. However, the Examiner has not provided a copy of U.S. provisional application serial no. 60/047,474 for Applicant's review. This reference is not readily available to Applicant. As such, Applicant is unable to fairly consider and rebut the Examiner's positions and/or interpretation taken with respect to U.S. provisional application serial no. 60/047,474. **If U.S. provisional application serial no. 60/047,474 is to be relied on in support of this rejection, the Examiner is respectfully requested to cite the provisional application of record and to provide a copy of the provisional application for Applicant's consideration.**

On page 5, lines 3-5 of the current Office Action, the Examiner has alleged that ion implantation is set in the Efland et al. reference to be carried out with an energy so that an accelerated oxidation during formation of the gate oxide layer is inhibited.

However, as noted above, the Efland et al. reference does not disclose or even remotely suggest setting energy of the implanting as described in column 3, lines 26-27 and/or the concept of accelerated oxidation. Applicant further respectfully submits that one of ordinary skill would not be led to the recited implant energy in connection with accelerated oxidation inhibition as alleged by the Examiner, because the prior art does not disclose or even remotely suggest these aspects even in a general sense.

Accordingly, Applicant respectfully submits that the method of manufacturing an LDMOS transistor of claim 1 distinguishes over the Efland et al. reference as relied upon by the Examiner, and that this rejection of claims 1, 5 and 6 is improper for at least these reasons. Applicant also respectfully submits that the methods of manufacturing an LDMOS transistor of respective independent claims 7 and 13 distinguish over the Efland et al. reference as relied upon by the Examiner, and that this rejection of claims 7, 11-13, 17 and 18 is also improper for at least somewhat similar reasons.

Claim Rejections-35 U.S.C. 103

Claims 2-4, 8-10 and 14-16 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Efland et al. reference. Applicant respectfully submits that the Examiner's reliance on the Efland et al. reference in connection with this rejection does not overcome the above noted deficiencies of the Efland et al. reference, and that this rejection is therefore improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to enter the above noted amendments, which have been made directly responsive to the rejection under 35 U.S.C. 112, second paragraph. Consideration and entry of the above noted amendments should not be an undue burden requiring further consideration and/or search. That is, the scope of the claims has not been changed.

Applicant also respectfully submits that the above noted amendments have not been made to further distinguish the claims over the relied upon prior art, and thus should not be construed as narrowing scope within the meaning of *Festo*.

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to August 7, 2003, for the period in which to file a response to the outstanding Office Action. The required fee of \$110.00 is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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